

[2885/77]

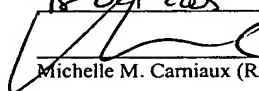
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s) : Martin VORBACH et al.
Serial No. : 10/764,159
Filing Date : January 23, 2004
For : METHOD OF HIERARCHICAL CACHING OF
CONFIGURATION DATA HAVING DATAFLOW
PROCESSORS AND MODULES HAVING TWO- OR
MULTIDIMENSIONAL PROGRAMMABLE CELL
STRUCTURE (FPGAs, DPGAs, etc.)

Group Art Unit : 2186
Examiner : Stephen C. Elmore
Confirmation No. : 8160

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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18 OCT 2005

Michelle M. Carniaux (Reg. No. 36,098)

**RESPONSE TO NOTICE OF DRAWING INCONSISTENCY WITH
SPECIFICATION**

SIR:

In response to the Notice of Drawing Inconsistency mailed September 29, 2005 in the
above-identified application, Applicant responds as follows:

Amendments to the Specification begin on page 2 of this paper.

Remarks begin on page 3 of this paper.